WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a semiconductor substrate;

a gate electrode formed on said semiconductor substrate via a gate insulating film;

a source region and a drain region of a first conductivity type formed on both sides of said gate electrode, respectively, in said semiconductor substrate; and

a punch-through stopper region of a second conductivity type formed in said semiconductor substrate such that said second conductivity type punch-through stopper region is located between said source region and said drain region at distances from said source region and said drain region and extends in a direction perpendicular to a principal surface of said semiconductor substrate,

wherein a concentration of an impurity element of the second conductivity type in said punch-through stopper region is set to be at least five times greater than a substrate impurity concentration between said source region and said drain region.

2. The semiconductor device as claimed in claim 1, wherein a bottom of the punch-through stopper region extends deeper than the source region and the drain region.

3. The semiconductor device as claimed in claim 1, wherein a top of the punch-through stopper region is located at a depth equal to or less than 10 nm from a surface of a channel formed in the semiconductor substrate.

4. The semiconductor device as claimed in claim 1, wherein a width of the punch-through stopper region is equal to or more than 10 nm.

5. The semiconductor device as claimed in claim 1, wherein, in the semiconductor substrate, a well of the second conductivity type is formed underneath the source region and the drain region at distances from the source region and the drain region, the source region and the drain region formed above said well are in a device region of the second conductivity type having the substrate impurity concentration, and the device region has a lower impurity concentration than said well as the substrate impurity concentration.

6. The semiconductor device as claimed in claim 1, wherein the punch-through stopper region is formed such that a bottom of the punch-through stopper region is located in the vicinity of the

well.

7. The semiconductor device as claimed in claim 1, wherein the punch-through stopper region is formed such that a bottom of the punch-through stopper region reaches the well.

8. The semiconductor device as claimed in claim 1, wherein the source region includes in a surface part thereof a first extension part extending along a surface of the semiconductor substrate in a direction toward the drain region, the drain region includes in a surface part thereof a second extension part extending along the surface of the semiconductor substrate in a direction toward the source region, a lower part of said first extension part forms a first pocket region extending toward said second extension part, and a lower part of said second extension region forms a second pocket region extending toward said first extension part.

9. The semiconductor device as claimed in claim 1, wherein a length of a gate is equal to or less than 0.1 μm.

10. The semiconductor device as claimed in claim 1, wherein the punch-through stopper region is doped by one of B and P.

11. A CMOS integrated circuit device, comprising:

a semiconductor substrate wherein a first device region and a second device region are defined, said first device region being formed with a first element of a first conductivity type including an inversion channel of a second conductivity type, and said second device region being formed with a second element of the second conductivity type including an inversion channel of the first conductivity type;

a first well of the first conductivity type having a higher impurity concentration and formed in said first device region at a distance from a surface of said semiconductor substrate;

a second well of the second conductivity type having a higher impurity concentration and formed in said second device region at a distance from the surface of said semiconductor substrate;

a first gate electrode formed on said semiconductor substrate via a first gate insulating film so as to correspond to said first device region;

a second gate electrode formed on said semiconductor substrate via a second gate insulating film so as to correspond to said second device region;

a first source region and a first drain region of the second conductivity type formed in said first device region in said semiconductor

substrate on both sides of said first gate electrode, respectively, at a distance from said first well;

a second source region and a second drain region of the first conductivity type formed in said second device region in said semiconductor substrate on both sides of said second gate electrode, respectively, at a distance from said second well;

a first punch-through stopper region of the first conductivity type formed between said first source region and said first drain region at distances from said first source region and said first drain region in said first device region in said semiconductor substrate and extending in a direction perpendicular to a principal surface of said semiconductor substrate; and

a second punch-through stopper region of the second conductivity type formed between said second source region and said second drain region at distances from said second source region and said second drain region in said second device region in said semiconductor substrate and extending in a direction perpendicular to the principal surface of said semiconductor substrate,

wherein a bottom of said first punch-through stopper region reaches in the vicinity of said first well, and

a bottom of said second punch-through stopper region reaches in the vicinity of said second well.

12. The CMOS integrated circuit device as claimed in claim 11, wherein the bottom of the first punch-through stopper region reaches the first well and the bottom of the second punch-through stopper

region reaches the second well.

13. The CMOS integrated circuit device as claimed in claim 11, wherein the first source region includes in a surface part thereof a first extension part extending along the surface of the semiconductor substrate in a direction toward the first drain region, the first drain region includes in a surface part thereof a second extension part extending along the surface of the semiconductor substrate in a direction toward the first source region, the second source region includes in a surface part thereof a third extension part extending along the surface of the semiconductor substrate in a direction toward the second drain region, and the second drain region includes in a surface part thereof a fourth extension part extending along the surface of the semiconductor substrate in a direction toward the second source region,

said first extension part includes a first pocket region formed by a lower part of said first extension part and extending toward said second extension part, and said second extension part includes a second pocket region formed by a lower part of said second extension part and extending toward said first extension part, and

said third extension part includes a third pocket region formed by a lower part of said third extension part and extending toward said fourth extension part, and said fourth extension part includes a fourth pocket region formed by a lower part of said fourth extension part and extending toward said third extension part.

14. The CMOS integrated circuit device as claimed in claim 11, wherein lengths of the first and second gate electrodes are equal to or less than 0.1 μm.

15. The CMOS integrated circuit device as claimed in claim 11, wherein the first punch-through stopper region is doped by one of B and P, and the second punch-through stopper region is doped by the other one of B and P.

16. A manufacturing method of a semiconductor device, comprising the steps of:

forming a dummy gate electrode on a surface of a semiconductor substrate so as to correspond to a channel region;

forming a source region and a drain region by introducing an impurity element of a first conductivity type into said semiconductor substrate using said dummy gate electrode as a mask;

forming an insulating film on the surface of said semiconductor substrate so as to cover said dummy gate electrode;

polishing said insulating film until said dummy gate is exposed;

removing said dummy gate electrode and forming an opening in said insulating film;

forming a sidewall film on a sidewall surface of said opening; and

forming a punch-through stopper region extending in a direction perpendicular to the surface of said semiconductor substrate by performing ion implantation of an impurity element of a second conductivity type into said semiconductor substrate at least twice with different acceleration voltages using said insulating film and said sidewall film as a mask,

wherein the step of forming said punch-through stopper region is performed later than the step of forming said source region and said drain region.

17. The manufacturing method of the semiconductor device as claimed in claim 16, wherein the step of forming the punch-through stopper region uses one of B and P as the impurity element of the second conductivity type.

18. The manufacturing method of the semiconductor device as claimed in claim 16, wherein, in the semiconductor substrate, a well of the second conductivity type is formed at a distance from the surface of the semiconductor substrate, the source region and the drain region are formed above said well of the second conductivity type at a distance from said well of the second conductivity type in the step of forming the source region and the drain region, and the step of forming the punch-through

stopper region is performed such that a bottom of the punch-through stopper region reaches in the vicinity of said well of the second conductivity type.

19. The manufacturing method of the semiconductor device as claimed in claim 16, wherein the step of forming the source region and the drain region further comprises the steps of:

forming a source extension region and a drain extension region of the first conductivity type in upper parts of the source region and the drain region, respectively, such that the source extension region and the drain extension region extend along the surface of the semiconductor substrate in a mutually opposing manner; and

forming, by performing ion implantation of an impurity element of the first conductivity type in an oblique direction using the dummy gate electrode as a mask, a first pocket region of the second conductivity type in a lower part of said source extension region and a second pocket region of the second conductivity type in a lower part of said drain extension region such that the first and second pocket regions extend in a mutually opposing manner.

20. A semiconductor device, comprising:

a semiconductor substrate;

a first device region of a semiconductor layer of a first conductivity type formed in said

semiconductor substrate;

a punch-through stopper layer of the first conductivity type formed in said first device region;

a second device region including a semiconductor layer of the first conductivity type formed on said punch-through stopper layer;

a trench formed in said second device region so as to cut across said punch-through stopper layer and expose a part of said first device region;

a gate insulating film formed on a surface of said trench so as to continuously extend from said second device region to said first device region;

a first diffusion region of a second conductivity type formed adjacent to said trench in said second device region;

a second diffusion region of the second conductivity type formed adjacent to said trench in said first device region; and

a gate electrode formed in said trench so as to cover said gate insulating film,

wherein said punch-through stopper layer has greater impurity concentration than said first and second device regions.